DATA SHEET

TDA4680
Video processor with automatic cut-off and white level control

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

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Video processor with automatic cut-off and white level control

TDA4680

FEATURES

- Operates from an 8 V DC supply
- Black level clamping of the colour difference, luminance and RGB input signals with coupling-capacitor DC level storage
- Two fully-controlled, analog RGB inputs, selected either by fast switch signals or via I^{2}C-bus
- Saturation, contrast and brightness adjustment via I^{2}C-bus
- Same RGB output black levels for Y/CD and RGB input signals
- Timing pulse generation from either a 2 or 3-level sandcastle pulse for clamping, horizontal and vertical synchronization, cut-off and white level timing pulses
- Automatic cut-off control with picture tube leakage current compensation
- Software-based automatic white level control or fixed white levels via I^{2}C-bus
- Cut-off and white level measurement pulses in the last 4 lines of the vertical blanking interval (I^{2}C-bus selection for PAL, SECAM, or NTSC, PAL-M)
- Increased RGB signal bandwidths for progressive scan and 100 Hz operation (selected via I^{2}C-bus)
- Two switch-on delays to prevent discolouration before steady-state operation
- Average beam current and peak drive limiting
- PAL/SECAM or NTSC matrix selection via I^{2}C-bus
- Three adjustable reference voltage levels (via I^{2}C-bus) for automatic cut-off and white level control
- Emitter-follower RGB output stages to drive the video output stages
- Hue control output for the TDA4555, TDA4650/T, TDA4655/T or TDA4657.

GENERAL DESCRIPTION

The TDA4680 is a monolithic integrated circuit with a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from multistandard colour decoders, TDA4555, TDA4650/T, TDA4655/T or TDA4657, Colour Transient Improvement (CTI) IC, TDA4565, Picture Signal Improvement (PSI) IC, TDA4670, or from a feature module.

The required input signals are:

- Luminance and negative colour difference signals
- 2 or 3-level sandcastle pulse for internal timing pulse generation
- I^{2}C-bus data and clock signals for microcontroller control.

Two sets of analog RGB colour signals can also be inserted, e.g. one from a peritelevision connector and the other from an on-screen display generator; both inputs are fully-controlled internally. The TDA4680 includes full I^{2}C-bus control of all parameters and functions with automatic cut-off and white level control of the picture tube cathode currents. It provides RGB output signals for the video output stages.

There is a very similar IC TDA4681 available. The only differences are in the NTSC matrix.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4680	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TDA4680WP	PLCC28	plastic leaded chip carrier; 28 leads	SOT261-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.2	8.0	8.8	V
I_P	supply current (pin 5)	–	85	–	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value)	–	0.45	–	V
$V_{6(p-p)}$	–(B – Y) input (peak-to-peak value)	–	1.33	–	V
$V_{7(p-p)}$	–(R – Y) input (peak-to-peak value)	–	1.05	–	V
V_{14}	3-level sandcastle pulse				
	H + V	–	2.5	–	V
	H	–	4.5	–	V
	BK	–	8.0	–	V
	2-level sandcastle pulse				
	H + V	–	2.5	–	V
	BK	–	4.5	–	V
$V_{i(p-p)}$	RGB input signals at pins 2, 3, 4, 10, 11 and 12 (peak-to-peak value)	–	0.7	–	V
$V_{o(b-w)}$	RGB outputs at pins 24, 22 and 20 (black-to-white value)	–	2.0	–	V
T_{amb}	operating ambient temperature	0	–	70	°C

BLOCK DIAGRAM

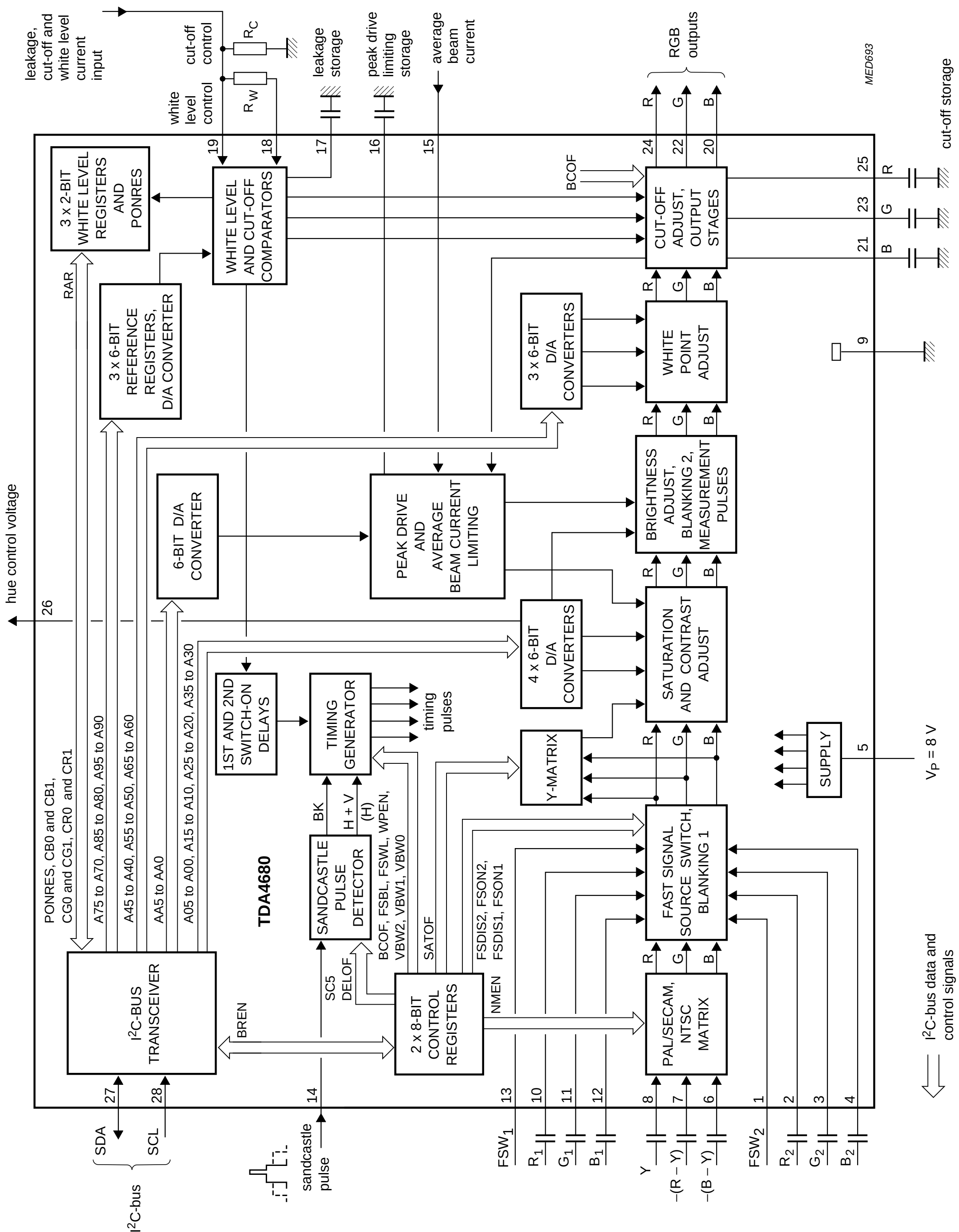


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_P	5	supply voltage
–(B – Y)	6	colour difference input –(B – Y)
–(R – Y)	7	colour difference input –(R – Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak drive limiting
C_L	17	storage capacitor for leakage current
WI	18	white level measurement input
CI	19	cut-off measurement input
B_O	20	blue output
C_B	21	blue cut-off storage capacitor
G_O	22	green output
C_G	23	green cut-off storage capacitor
R_O	24	red output
C_R	25	red cut-off storage capacitor
HUE	26	hue control output
SDA	27	I^2C-bus serial data input/output
SCL	28	I^2C-bus serial clock input

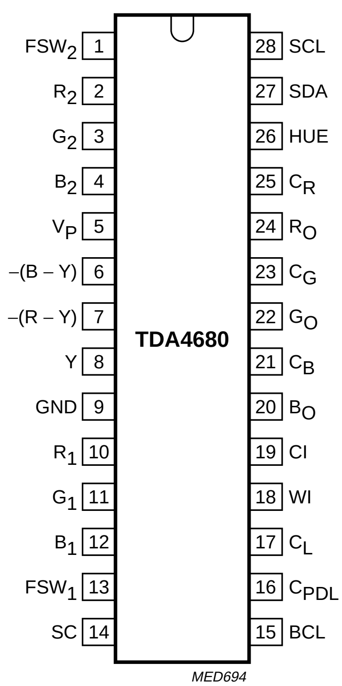


Fig.2 Pin configuration for DIP-version.

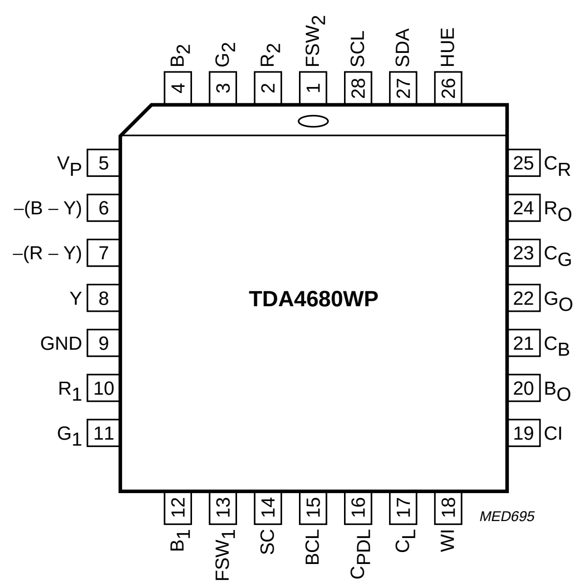


Fig.3 Pin configuration for PLCC-version.

I²C-BUS

Control

The I²C-bus transmitter/receiver provides the data bytes to select and adjust the following functions and parameters:

- Brightness adjust
- Saturation adjust
- Contrast adjust
- Hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- Peak drive limiting
- Selection of the vertical blanking interval and measurement lines for cut-off and white level control according to transmission standard
- Selects either 3-level or 2-level (5 V) sandcastle pulse
- Enables/disables input clamping pulse delay
- Enables/disables white level control
- Enables cut-off control; enables output clamping
- Enables/disables full screen white level
- Enables/disables full screen black level
- Selects either PAL/SECAM or NTSC matrix
- Enables saturation adjust; enables nominal saturation
- Enables/disables synchronization of the execution of I²C-bus commands with the vertical blanking interval
- Reads the result of the comparison of the nominal and actual RGB signal levels for automatic white level control.

I²C-bustransmitter/receiver and data transfer

I²C-BUS SPECIFICATION

The I²C-bus is a bidirectional, two-wire, serial data bus for intercommunication between ICs in a system.
The microcontroller transmits/receives data from the I²C-bus transceiver in the TDA4680 over the serial data line SDA (pin 27) synchronized by the serial clock line SCL (pin 28). Both lines are normally connected to a positive voltage supply through pull-up resistors. Data is transferred when the SCL line is LOW. When SCL is HIGH the serial data line SDA must be stable. A HIGH-to-LOW transition of the SDA line when SCL is HIGH is defined as a START bit. A LOW-to-HIGH transition of the SDA line when SCL is HIGH is defined as a STOP bit.
Each transmission must start with a START bit and end with a STOP bit. The bus is busy after a START bit and is only free again after a STOP bit has been transmitted.

I²C-BUS RECEIVER (MICROCONTROLLER WRITE MODE)

Each transmission to/from the I²C-bus transceiver consists of at least three bytes following the START bit. Each byte is acknowledged by an acknowledge bit immediately following each byte. The first byte is the Module Address (MAD) byte, also called slave address byte. This consists of the module address, 1000100 for the TDA4680, plus the R/$\overline{W}$ bit (see Fig.4). When the TDA4680 is a slave receiver (R/$\overline{W}$ = 0) the module address byte is 10001000 (88H). When the TDA4680 is a slave transmitter (R/$\overline{W}$ = 1) the module address byte is 10001001 (89H).

The length of a data transmission is unrestricted, but the module address and the correct sub-address must be transmitted before the data byte(s). The order of data transmission is shown in Figs 5 and 6.
Without auto-increment (BREN = 0 or 1) the module address (MAD) byte is followed by a Sub-Address (SAD) byte and one data byte only (see Fig.5).

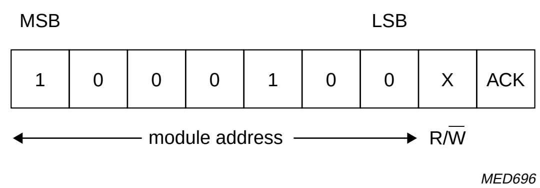


Fig.4 The module address byte.

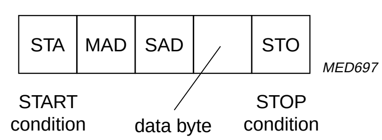


Fig.5 Data transmission without auto-increment (BREN = 0 or 1).

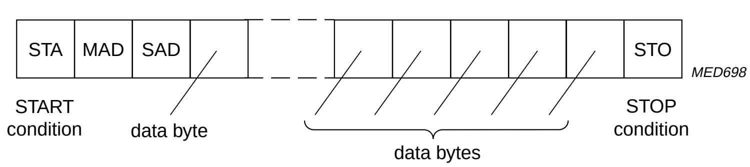


Fig.6 Data transmission with auto-increment (BREN = 0).

AUTO-INCREMENT

The auto-increment format enables quick slave receiver initialization by one transmission, when the I^2C-bus control bit BREN = 0 (see control register bits of Table 1).
If BREN = 1 auto-increment is not possible.

If the auto-increment format is selected, the MAD byte is followed by a SAD byte and by the data bytes of consecutive sub-addresses (Fig.6).

All sub-addresses from 00H to 0FH are automatically incremented, the sub-address counter wraps round from 0FH to 00H. Reserved sub-addresses 0BH, 0EH and 0FH are treated as legal but have no effect. Sub-addresses outside the range 00H and 0FH are not acknowledged by the device and neither auto-increment nor any other internal operation takes place (for versions V1 to V5 sub-addresses outside the range 00H and 0FH are acknowledged but neither auto-increment nor any other internal operation takes place).

Sub-addresses are stored in the TDA4680 to address the following parameters and functions (see Table 1):

- Brightness adjust
- Saturation adjust
- Contrast adjust
- Hue control voltage
- RGB gain adjust
- RGB reference voltage levels
- Peak drive limiting adjust
- Control register functions.

The data bytes D7 to D0 (see Table 1) provide the data of the parameters and functions for video processing.

CONTROL REGISTER 1

VBWx (Vertical Blanking Window):

x = 0, 1 or 2. VBWx selects the vertical blanking interval and positions the measurement lines for cut-off and white level control.

The actual lines in the vertical blanking interval after the start of the vertical pulses selected as measurement lines for cut-off and white level control are shown in Table 2.

The standards marked with (*) are for progressive line scan at double line frequency ($2f_L$), i.e. approximately 31 kHz.

NMEN (NTSC Matrix Enable):

0 = PAL/SECAM matrix

1 = NTSC matrix.

WPEN (White Pulse Enable):

0 = white measuring pulse disabled

1 = white measuring pulse enabled.

BREN (Buffer Register Enable):

0 = new data is executed as soon as it is received

1 = data is stored in buffer registers and is transferred to the data registers during the next vertical blanking interval.

The I^2C-bus transceiver does not accept any new data until this data is transferred into the data registers.

DELOF (Delay Off) delays the leading edge of clamping pulses:

0 = delay enabled

1 = delay disabled.

SC5 (SandCastle 5 V):

0 = 3-level sandcastle pulse

1 = 2-level (5 V) sandcastle pulse.

CONTROL REGISTER 2

FSON2 (Fast Switch 2 ON)

FSDIS2 (Fast Switch 2 Disable)

FSON1 (Fast Switch 1 ON)

FSDIS1 (Fast Switch 1 Disable)

The RGB input signals are selected by FSON2 and FSON1 or FSW_2 and FSW_1:

- FSON2 has priority over FSON1
- FSW_2 has priority over FSW_1
- FSDIS1 and FSDIS2 disable FSW_1 and FSW_2 (see Table 3).

BCOF (Black level Control Off):

0 = automatic cut-off control enabled

1 = automatic cut-off control disabled; RGB outputs are clamped to fixed DC levels.

FSBL (Full Screen Black Level):

0 = normal mode

1 = full screen black level (cut-off measurement level during full field).

FSWL (Full Screen White Level):

0 = normal mode

1 = full screen white level (white measurement level during full field).

SATOF (Saturation control Off):

0 = saturation control enabled

1 = saturation control disabled, nominal saturation enabled.

I²C-BUS TRANSMITTER (MICROCONTROLLER READ MODE)

As an I²C-bus transmitter, R/$\overline{W}$ = 1, the TDA4680 sends a data byte from the status register to the microcontroller. The data byte consists of following bits: PONRES, CB1, CB0, CG1, CG0, CR1, CR0 and 0, where PONRES is the most significant bit.

PONRES (Power On Reset) monitors the state of TDA4680's supply voltage:

0 = normal operation

1 = supply voltage has dropped below approximately 6.0 V (usually occurs when the TV receiver is switched on or the supply voltage was interrupted).

When PONRES changes state from a logic LOW to a logic HIGH all data and function bits are set to logic LOW.

2-BIT WHITE LEVEL ERROR SIGNAL (see Table 4)

CB1, CB0 = 2-bit white level of the blue channel.

CG1, CG0 = 2-bit white level of the green channel.

CR1, CR0 = 2-bit white level of the red channel.

Table 1 Sub-address (SAD) and data bytes; note 1

FUNCTION	SAD (HEX)	MSB							LSB
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Brightness	00	0	0	A05	A04	A03	A02	A01	A00
Saturation	01	0	0	A15	A14	A13	A12	A11	A10
Contrast	02	0	0	A25	A24	A23	A22	A21	A20
Hue control voltage	03	0	0	A35	A34	A33	A32	A31	A30
Red gain	04	0	0	A45	A44	A43	A42	A41	A40
Green gain	05	0	0	A55	A54	A53	A52	A51	A50
Blue gain	06	0	0	A65	A64	A63	A62	A61	A60
Red level reference	07	0	0	A75	A74	A73	A72	A71	A70
Green level reference	08	0	0	A85	A84	A83	A82	A81	A80
Blue level reference	09	0	0	A95	A94	A93	A92	A91	A90
Peak drive limit	0A	0	0	AA5	AA4	AA3	AA2	AA1	AA0
Reserved	0B	X	X	X	X	X	X	X	X
Control register 1	0C	SC5	DELOF	BREN	WPEN	NMEN	VBW2	VBW1	VBW0
Control register 2	0D	SATOF	FSWL	FSBL	BCOF	FSDIS2	FSON2	FSDIS1	FSON1
Reserved	0E	X	X	X	X	X	X	X	X
Reserved	0F	X	X	X	X	X	X	X	X

Note

1. X = don't care.

Table 2 Cut-off and white level measurement lines; notes 1 to 3

VBW2	VBW1	VBW0	R	G	B	WHITE	STANDARD
0	0	0	19	20	21	22	PAL/SECAM
0	0	1	16	17	18	19	NTSC/PAL M
0	1	0	22	23	24	25	PAL/SECAM (EB)
1	0	0	38, 39	40, 41	42, 43	44, 45	PAL*/SECAM*
1	0	1	32, 33	34, 35	36, 37	38, 39	NTSC*/PAL M*
1	1	0	44, 45	46, 47	48, 49	50, 51	PAL*/SECAM* (EB)

Notes

1. The line numbers given are those of the horizontal pulse counts after the start of the vertical component of the sandcastle pulse.
2. * line frequency of approximately 31 kHz.
3. (EB) is extended blanking.

Table 3 Signal input selection by the fast source switches; notes 1 to 4

I^2C-BUS CONTROL BITS				ANALOG SWITCH SIGNALS		INPUT SELECTED		
FSON2	**FSDIS2**	**FSON1**	**FSDIS1**	**FSW_2 (PIN 1)**	**FSW_1 (PIN 13)**	**RGB_2**	**RGB_1**	**Y/CD**
L	L	L	L	L	L			ON
				L	H		ON	
				H	X	ON		
L	L	L	H	L	X			ON
				H	X	ON		
L	L	H	X	L	X		ON	
				H	X	ON		
L	H	L	L	X	L			ON
				X	H		ON	
L	H	L	H	X	X			ON
L	H	H	X	X	X		ON	
H	X	X	X	X	X	ON		

Notes

1. H: logical HIGH implies that the voltage >0.9 V.
2. L: logical LOW implies that the voltage <0.4 V.
3. X = don’t care.
4. ON indicates the selected input signal.

Table 4 2-bit white level error signals; bits CX1 and CX0

CX1	CX0	INTERPRETATION
0	0	RAR (Reset-After-Read): no new measurements since last read
1	0	actual (measured) white level less than the tolerance range
1	1	actual (measured) white level within the tolerance range
0	1	actual (measured) white level greater than the tolerance range

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 5)	–	8.8	V
V_i	input voltage (pins 1 to 8, 10 to 13, 16, 21, 23 and 25)	–0.1	$+V_P$	V
	input voltage (pins 14, 15, 18 and 19)	–0.7	V_P + 0.7	V
	input voltage (pins 27 and 28)	–0.1	+8.8	V
I_{av}	average current (pins 20, 22 and 24)	+4	–10	mA
I_M	peak current (pins 20, 22 and 24)	+4	–20	mA
I_{18}	input current	0	2	mA
I_{26}	output current	+0.5	–8	mA
T_{stg}	storage temperature	–20	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
P_{tot}	total power dissipation			
	SOT117-1	–	1.2	W
	SOT261-2	–	1.0	W

CHARACTERISTICS

All voltages are measured in test circuit of Fig.10 with respect to GND (pin 9); V_P = 8.0 V; T_{amb} = 25 °C; nominal signal amplitudes (black-to-white) at output pins 24, 22 and 20; nominal settings of brightness, contrast, saturation and white level control; without beam current or peak drive limiting; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 5)						
V_P	supply voltage		7.2	8.0	8.8	V
I_P	supply current		–	85	110	mA
Colour difference inputs [–(B – Y): pin 6; –(R – Y): pin 7]						
$V_{6(p-p)}$	–(B – Y) input (peak-to-peak value)	notes 1 and 2	–	1.33	–	V
$V_{7(p-p)}$	–(R – Y) signal (peak-to-peak value)	notes 1 and 2	–	1.05	–	V
$V_{6,7}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$\|I_{6,7}\|$	input current	during line scan	–	–	0.15	µA
		at black level clamping	100	–	–	µA
$R_{6,7}$	AC input resistance		10	–	–	MΩ
Luminance/sync (VBS; Y: pin 8)						
$V_{i(p-p)}$	luminance input voltage at pin 8 (peak-to-peak value)	note 2	–	0.45	–	V
$V_{8(bias)}$	internal DC bias voltage	at black level clamping	–	3.1	–	V
$\|I_8\|$	input current	during line scan	–	–	0.15	µA
		at black level clamping	100	–	–	µA
R_8	AC input resistance		10	–	–	MΩ
RGB input 1 (R_1: pin 10; G_1: pin 11; B_1: pin 12)						
$V_{i(p-p)}$	input voltage at pins 10, 11 and 12 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{10/11/12(bias)}$	internal DC bias voltage	at black level clamping	–	5.4	–	V
$\|I_{10/11/12}\|$	input current	during line scan	–	–	0.15	µA
		at black level clamping	100	–	–	µA
$R_{10/11/12}$	AC input resistance		10	–	–	MΩ
RGB input 2 (R_2: pin 2, G_2: pin 3, B_2: pin 4)						
$V_{i(p-p)}$	input voltage at pins 2, 3 and 4 (peak-to-peak value)	note 2	–	0.7	–	V
$V_{2/3/4}$	internal DC bias voltage	at black level clamping	–	5.4	–	V
$\|I_{2/3/4}\|$	input current	during line scan	–	–	0.15	µA
		at black level clamping	100	–	–	µA
$R_{2/3/4}$	AC input resistance		10	–	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Fast signal switch FSW_1 (pin 13) to select Y, CD or R_1, G_1, B_1 inputs (control bits: see Table 3)						
V_{13}	voltage to select Y and CD		–	–	0.4	V
	voltage range to select R_1, G_1, B_1		0.9	–	5.0	V
R_{13}	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Fast signal switch FSW_2 (pin 1) to select Y, CD/R_1, G_1, B_1 or R_2, G_2, B_2 inputs (control bits: see Table 3)						
V_1	voltage to select Y, CD/R_1, G_1, B_1		–	–	0.4	V
	voltage to select R_2, G_2, B_2		0.9	–	5.0	V
R_1	internal resistance to ground		–	4.0	–	kΩ
Δt	difference between transit times for signal switching and signal insertion		–	–	10	ns
Saturation adjust [acts on internal RGB signals under I^2C-bus control; sub-address 01H (bit resolution 1.5% of maximum saturation); data byte 3FH for maximum saturation, data byte 23H for nominal saturation and data byte 00H for minimum saturation]						
d_s	saturation below maximum	at 23H	–	5	–	dB
		at 00H; f = 100 kHz	–	50	–	dB
Contrast adjust [acts on internal RGB signals under I^2C-bus control; sub-address 02H (bit resolution 1.5% of maximum contrast); data byte 3FH for maximum contrast, data byte 2CH for nominal contrast and data byte 00H for minimum contrast]						
d_c	contrast below maximum	at 2CH	–	3	–	dB
		at 00H	–	22	–	dB
Brightness adjust [acts on internal RGB signals under I^2C-bus control; sub-address 00H (bit resolution 1.5% of brightness range); data byte 3FH for maximum brightness, data byte 27H for nominal brightness and data byte 00H for minimum brightness]						
d_{br}	black level shift of nominal signal amplitude referred to cut-off measurement level	at 3FH	–	30	–	%
		at 00H	–	–50	–	%
White potentiometers [under I^2C-bus control; sub-addresses 04H (red), 05H (green) and 06H (blue); data byte 3FH for maximum gain; data byte 22H for nominal gain and data byte 00H for minimum gain]; note 3						
ΔG_v	relative to nominal gain					
	increase of AC gain	at 3FH	–	60	–	%
	decrease of AC gain	at 00H	–	60	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RGB outputs (pins 24, 22 and 20; positive going output signals and no peak drive limitation; sub-address 0AH = 3FH); note 4						
$V_{o(b\text{-}w)}$	nominal output signals (black-to-white value)		–	2.0	–	V
	maximum output signals (black-to-white value)		3.2	–	–	V
ΔV_o	spread between RGB output signals		–	–	10	%
V_o	output voltages		6.8	–	0.8	V
$V_{24,22,20}$	voltage of cut-off measurement line	output clamping (BCOF = 1)	2.3	2.5	2.7	V
I_{int}	internal current sources		–	5.0	–	mA
R_o	output resistance		–	65	110	Ω
Frequency response						
d	frequency response of Y path (from pin 8 to pins 24, 22, 20)	f = 10 MHz	–	–	3	dB
	frequency response of CD path (from pins 7 to 24 and 6 to 20)	f = 8 MHz	–	–	3	dB
	frequency response of RGB_1 path (from pins 10 to 24, 11 to 22 and 12 to 20)	f = 10 MHz	–	–	3	dB
	frequency response of RGB_2 path (from pins 2 to 24, 3 to 22 and 4 to 20)	f = 10 MHz	–	–	3	dB
Sandcastle pulse detector (pin 14)						
CONTROL BIT SC5 = 0; 3-LEVEL; notes 5 and 6						
V_{14}	sandcastle pulse voltage					
	for horizontal and vertical blanking pulses		2.0	2.5	3.0	V
	for horizontal pulses (line count)		4.0	4.5	5.0	V
	for burst key pulses		6.3	–	$V_P + 0.7$	V
CONTROL BIT SC5 = 1; 2-LEVEL; note 5						
V_{14}	sandcastle pulse voltage					
	for horizontal and vertical blanking pulses		2.0	2.5	3.0	V
	for burst key pulses		4.0	4.5	$V_P + 0.7$	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
GENERAL						
I_{14}	input current	V_{14} < 0.5 V	–100	–	–	µA
t_d	leading edge delay of the clamping pulse	control bit DELOF = 0	–	1.5	–	µs
		control bit DELOF = 1	–	0	–	µs
t_{BK}	required burst key pulse time	control bit DELOF = 0; normally used with f_L	3	–	–	µs
		control bit DELOF = 1; normally used with $2f_L$	1.5	–	–	µs
n_{pulse}	required horizontal or burst key pulses during vertical blanking interval	e.g. at interlace scan (VBW2 = 0)	4	–	29	–
		e.g. at progressive line scan (VBW2 = 1)	8	–	57	–
Average beam current limiting (pin 15); note 7						
$V_{c(15)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(15)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(15)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(15)}$	voltage difference for full brightness reduction		–	–1.6	–	V
Peak drive limiting voltage [pin 16; internal peak drive limiting level (V_{pdl}) acts on RGB outputs under I^2C-bus control; sub-address 0AH]; note 8						
$V_{20/22/24}$	RGB output voltages	at 00H	–	–	3.0	V
		at 3FH	6.5	–	–	V
I_{16}	charge current		–	–1	–	µA
	discharge current	during peak white	–	5	–	mA
V_{16}	internal voltage limitation		4.5	–	–	V
$V_{c(16)}$	contrast reduction starting voltage		–	4.0	–	V
$\Delta V_{c(16)}$	voltage difference for full contrast reduction		–	–2.0	–	V
$V_{br(16)}$	brightness reduction starting voltage		–	2.5	–	V
$\Delta V_{br(16)}$	voltage difference for full brightness reduction		–	–1.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Automatic cut-off and white level control (pins 19 and 18); notes 9 to 11; see Fig.8						
V_{19}	permissible voltage (also during scanning period)		–	–	V_P – 1.4	V
I_{19}	output current		–	–	–140	μA
	input current		150	–	–	μA
	additional input current	only during warming up	–	0.5	–	mA
$V_{24,22,20}$	warming up amplitude (under I^{2}C-bus control; sub-address 0AH)	switch-on delay 1	–	V_{pdl} – 0.7	–	V
$V_{19(th)}$	voltage threshold for picture tube cathode warming up	switch-on delay 1	–	5.0	–	V
V_{ref}	internally controlled voltage	during leakage measurement period	–	3.0	–	V
DATA BYTE 07H FOR RED REFERENCE LEVEL, DATA BYTE 08H FOR GREEN REFERENCE LEVEL AND DATA BYTE 09H FOR BLUE REFERENCE LEVEL						
ΔV_{19}	difference between V_{MEAS} (cut-off or white level measurement voltage) and V_{ref}	3FH (maximum V_{MEAS})	1.5	–	–	V
		20H (nominal V_{MEAS})	–	1.0	–	V
		00H (minimum V_{MEAS})	–	–	0.5	V
I_{18}	input current	white level measurement	–	–	800	μA
R_{18}	internal resistance	to V_{ref}; $I_{18} \leq 800$ μA	–	100	–	Ω
ΔV_{19}	white level register (measured value within tolerance range)	white level measurement	–	250	–	mV
Storage of cut-off control voltage/output clamping voltage (pins 25, 23 and 21)						
$\lvert I_{21/23/25} \rvert$	charge and discharge currents	during cut-off measurement lines	–	0.3	–	mA
	input currents of storage inputs	outside measurement time	–	–	0.1	μA
Storage of leakage information (pin 17)						
$\lvert I_{17} \rvert$	charge and discharge currents	during leakage measurement period	–	0.4	–	mA
	leakage current	outside time LM	–	–	0.1	μA
V_{17}	voltage for reset to switch-on below		–	–	3.0	V
Hue control (under I^{2}C-bus control; sub-address 03H; data byte 3FH for maximum voltage; data byte 20H for nominal voltage and data byte 00H for minimum voltage); note 12						
V_{26}	output voltage	at 3FH	4.8	–	–	V
		at 20H	–	3.0	–	V
		at 00H	–	–	1.0	V
I_{int}	current of the internal current source at pin 26		500	–	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus transceiver clock SCL (pin 28)						
f_{SCL}	input frequency range		0	–	100	kHz
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current	V_{28} = 0.4 V	–10	–	–	µA
I_{IH}	HIGH level input current		–	–	10	µA
t_L	clock pulse LOW		4.7	–	–	µs
t_H	clock pulse HIGH		4.0	–	–	µs
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
I²C-bus transceiver data input/output SDA (pin 27)						
V_{IL}	LOW level input voltage		–	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	6.0	V
I_{IL}	LOW level input current	V_{27} = 0.4 V	–10	–	–	µA
I_{IH}	HIGH level input current		–	–	10	µA
I_{OL}	LOW level output current	V_{27} = 0.4 V	3.0	–	–	mA
t_r	rise time		–	–	1.0	µs
t_f	fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		0.25	–	–	µs

Notes to the characteristics

1. The values of the –(B – Y) and –(R – Y) colour difference input signals are for a 75% colour-bar signal.
2. The pins are capacitively coupled to a low ohmic source, with a recommended maximum output impedance of 600 Ω.
3. The white potentiometers affect the amplitudes of the RGB output signals including the white measurement pulses.
4. The RGB outputs at pins 24, 22 and 20 are emitter followers with current sources.
5. Sandcastle pulses are compared with internal threshold voltages independent of V_P. The threshold voltages separate the components of the sandcastle pulse. The particular component is generated when the voltage on pin 14 exceeds the defined internal threshold voltage.
   The internal threshold voltages (control bit SC5 = 0) are:
   - 1.5 V for horizontal and vertical blanking pulses
   - 3.5 V for horizontal pulses
   - 6.0 V for the burst key pulse.

   The internal threshold voltages (control bit SC5 = 1) are:
   - 1.5 V for horizontal and vertical blanking pulses
   - 3.5 V for the burst key pulse.
6. A sandcastle pulse with a maximum voltage equal to (V_P + 0.7 V) is obtained by limiting a 12 V sandcastle pulse.
7. Average beam current limiting reduces the contrast, at minimum contrast it reduces the brightness.
8. Peak drive limiting reduces the RGB outputs by reducing the contrast, at minimum contrast it reduces the brightness. The maximum RGB outputs are determined via the I²C-bus under sub-address 0AH. When an RGB output exceeds the maximum voltage, peak drive limiting is delayed by one horizontal line.

9. The vertical blanking interval is defined by a vertical pulse which contains 4 (8) or more horizontal pulses; it begins with the start of the vertical pulse and ends with the end of the white measuring line. If the vertical pulse is longer than the selected vertical blanking window the blanking period ends with the end of the complete line after the end of the vertical pulse. The counter cycle time is 31 (63) horizontal pulses. If the vertical pulse contains more than 29 (57) horizontal pulses, the black level storage capacitors will be discharged while all signals are blanked. During leakage current measurement, the RGB channels are blanked to ultra-black level. During cut-off measurement one channel is set to the measurement pulse level, the other channels are blanked to ultra-black. Since the brightness adjust shifts the colour signal relative to the black level, the brightness adjust is disabled during the vertical blanking interval (see Figs 7 and 8).
10. During picture cathode warming up (first switch-on delay) the RGB outputs (pins 24, 22 and 20) are blanked to the ultra-black level during line scan. During the vertical blanking interval a white-level monitor pulse is fed out on the RGB outputs and the cathode currents are measured. When the voltage threshold on pin 19 is greater than 5.0 V, the monitor pulse is switched off and cut-off and white level control are activated (second switch-on delay). As soon as cut-off control stabilizes, RGB output blanking is removed.
11. Range of cut-off measurement level at the RGB outputs is 1 to 5 V. The recommended value is 3 V.
12. The hue control output at pin 26 is an emitter follower with current source.

Table 5 Demodulator axes and amplification factors

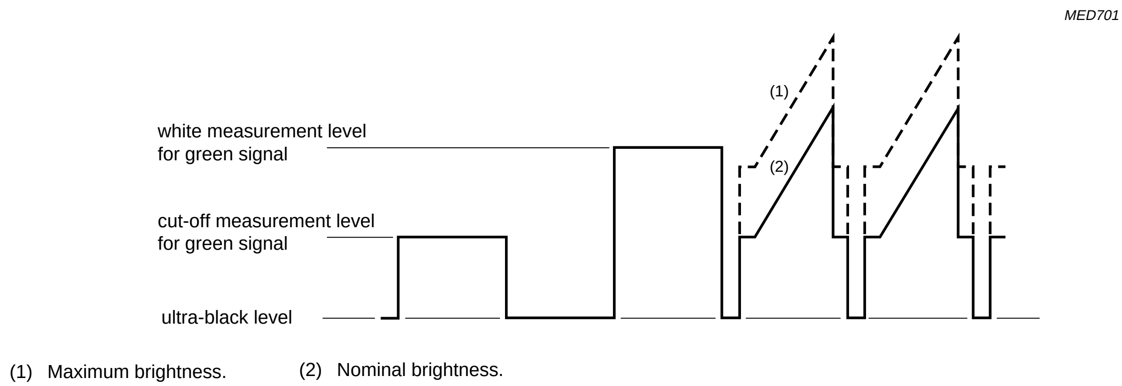
PARAMETER	NTSC	PAL
(B – Y)* demodulator axis	0°	0°
(R – Y)* demodulator axis	115°	90°
(R – Y)* amplification factor	1.97	1.14
(B – Y)* amplification factor	2.03	2.03

Table 6 PAL/SECAM and NTSC matrix; notes 1 and 2

MATRIX	NMEN
PAL/SECAM	0
NTSC	1

Notes

1. PAL/SECAM signals are matrixed by the equation: $V_{G-Y} = -0.51V_{R-Y} - 0.19V_{B-Y}$
NTSC signals are matrixed by the equations (hue phase shift of –5 degrees):
$V_{R-Y*} = 1.57V_{R-Y} - 0.41V_{B-Y}$; $V_{G-Y*} = -0.43V_{R-Y} - 0.11V_{B-Y}$; $V_{B-Y*} = V_{B-Y}$
In the matrix equations: V_{R-Y} and V_{B-Y} are conventional PAL demodulation axes and amplitudes at the output of the NTSC demodulator. V_{G-Y*}, V_{R-Y*} and V_{B-Y*} are the NTSC-modified colour difference signals; this is equivalent to the demodulator axes and amplification factors shown in Table 5. $V_{G-Y*} = -0.27V_{R-Y*} - 0.22V_{B-Y*}$.
2. The vertical blanking interval is selected via the I^2C-bus (see Table 2 and Fig.8). Vertical blanking is determined by the vertical component of the sandcastle pulse; this vertical component has priority when it is longer than the vertical blanking interval of the transmission standard.



(1) Maximum brightness. (2) Nominal brightness.

Fig.7 Cut-off and white level measurement pulses.

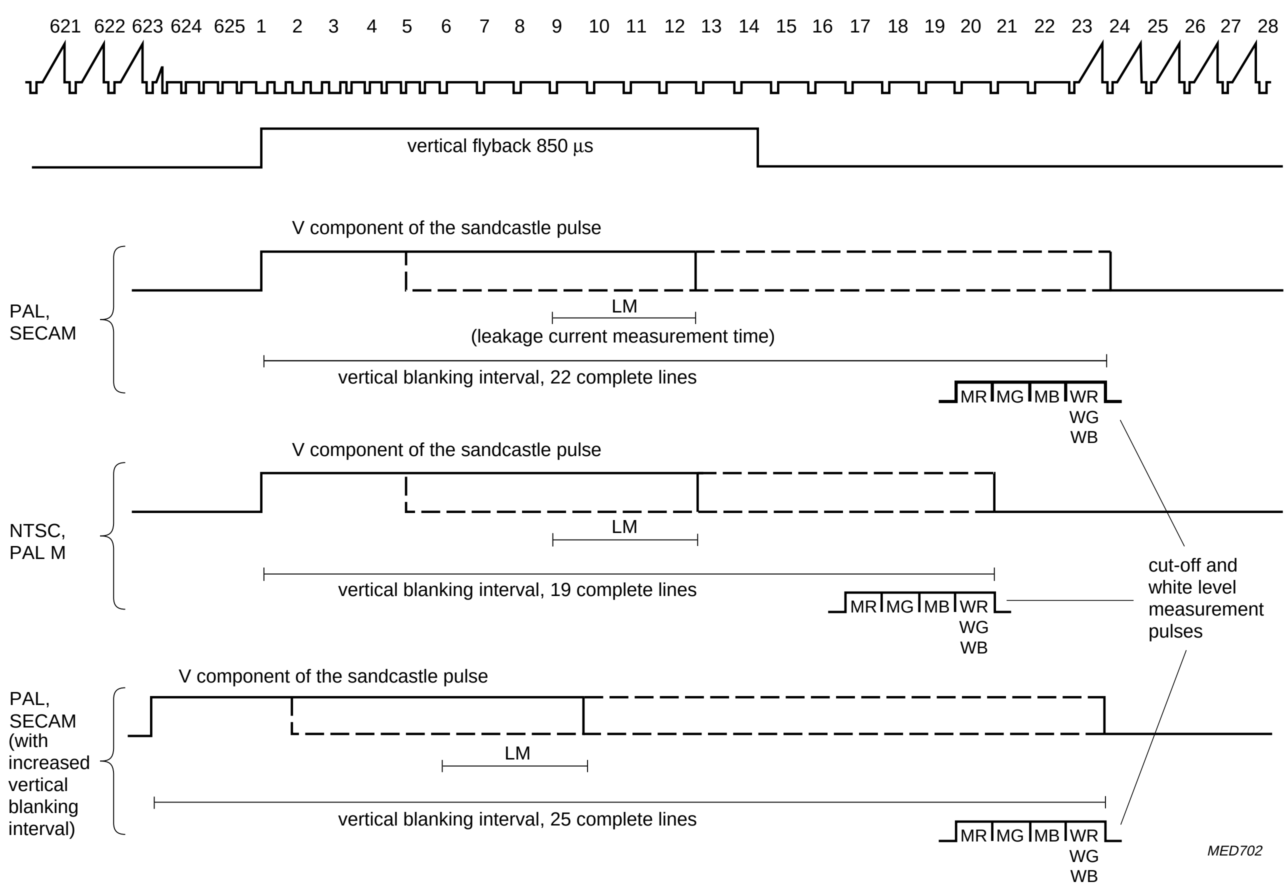


Fig.8 Leakage current, cut-off and white level current measurement timing diagram.

Video processor with automatic cut-off and white level control

TDA4680

INTERNAL PIN CONFIGURATION

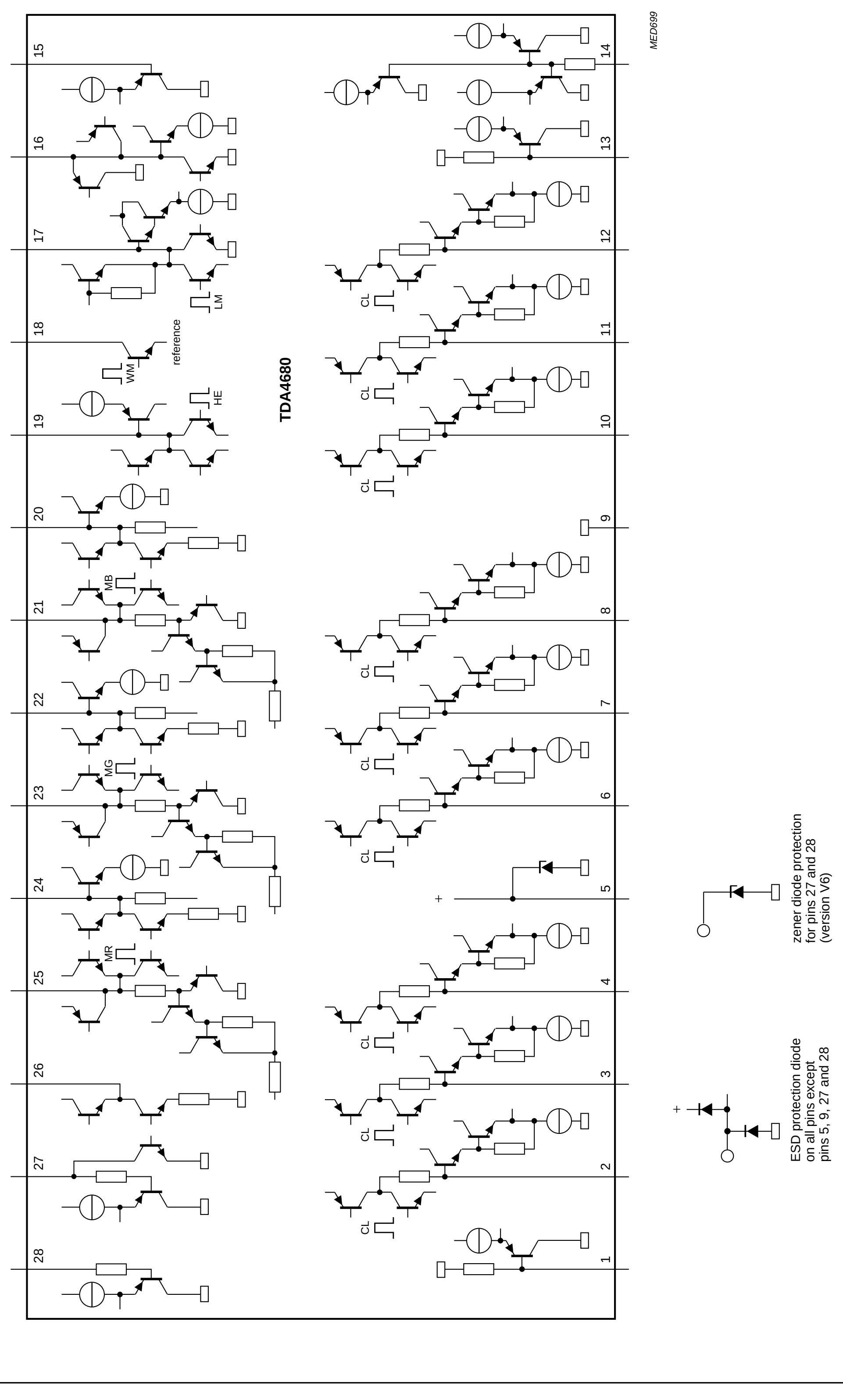
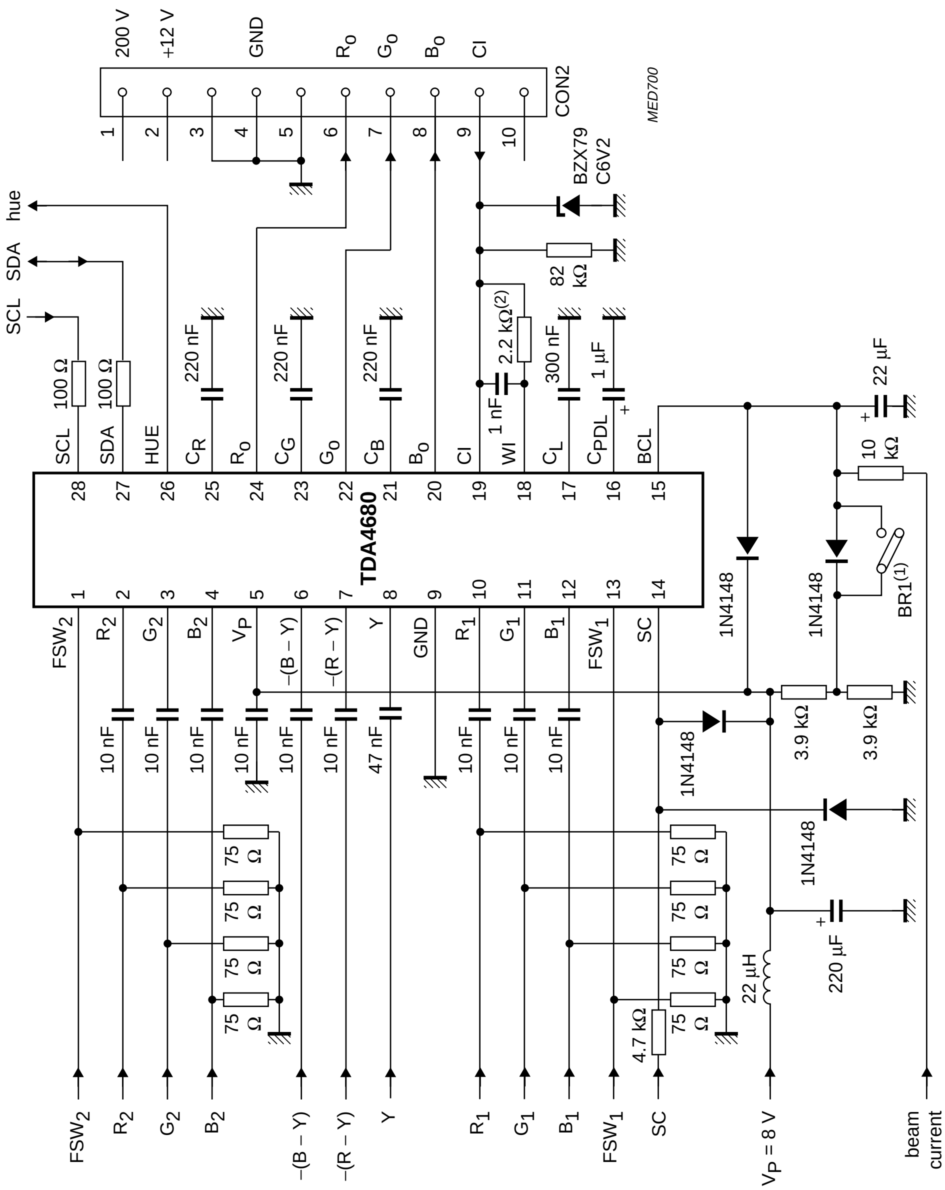


Fig.9 Internal circuits.

TEST AND APPLICATION INFORMATION



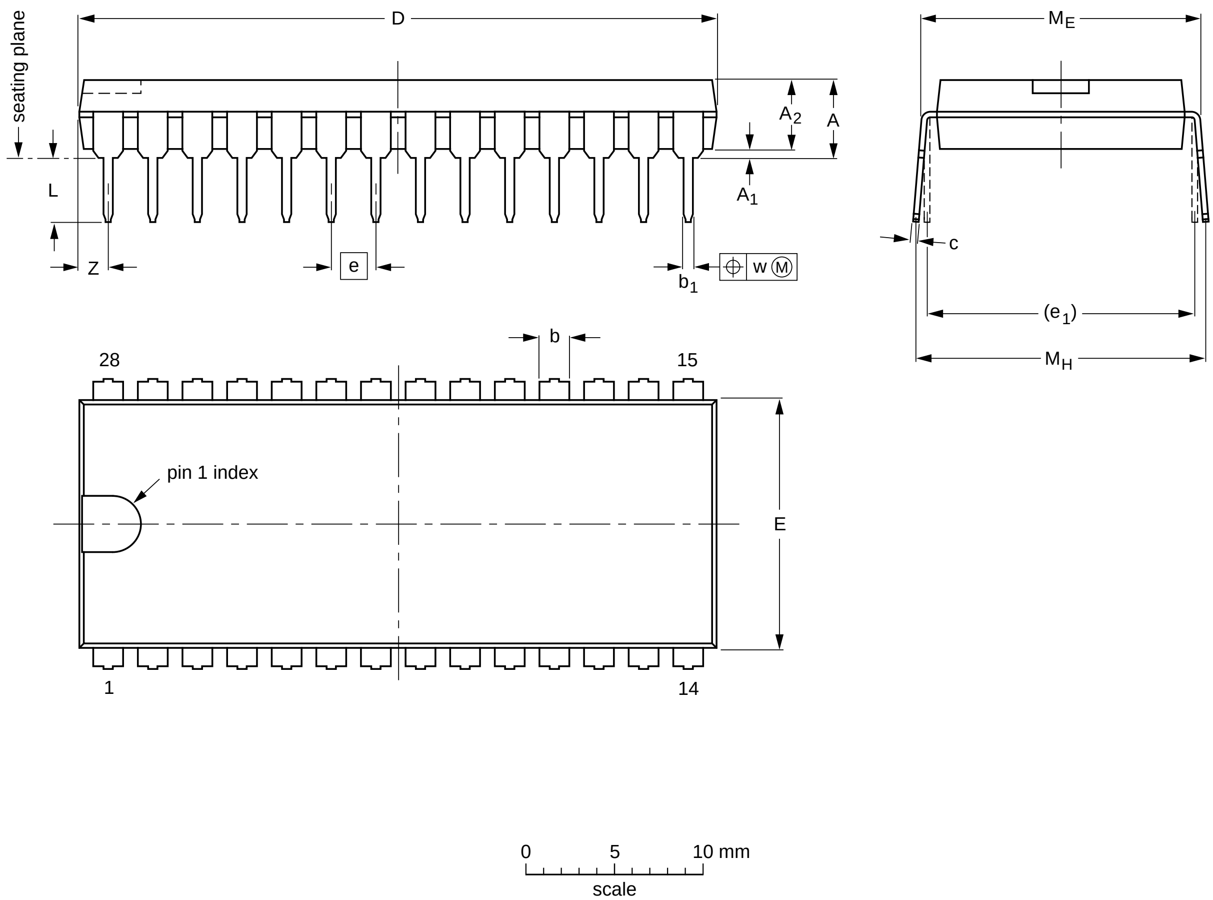
(1) Insert link BR1 if average beam current is not required.

(2) Value depends on video output current stages and picture tube.

Fig.10 Test and application circuit.

PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

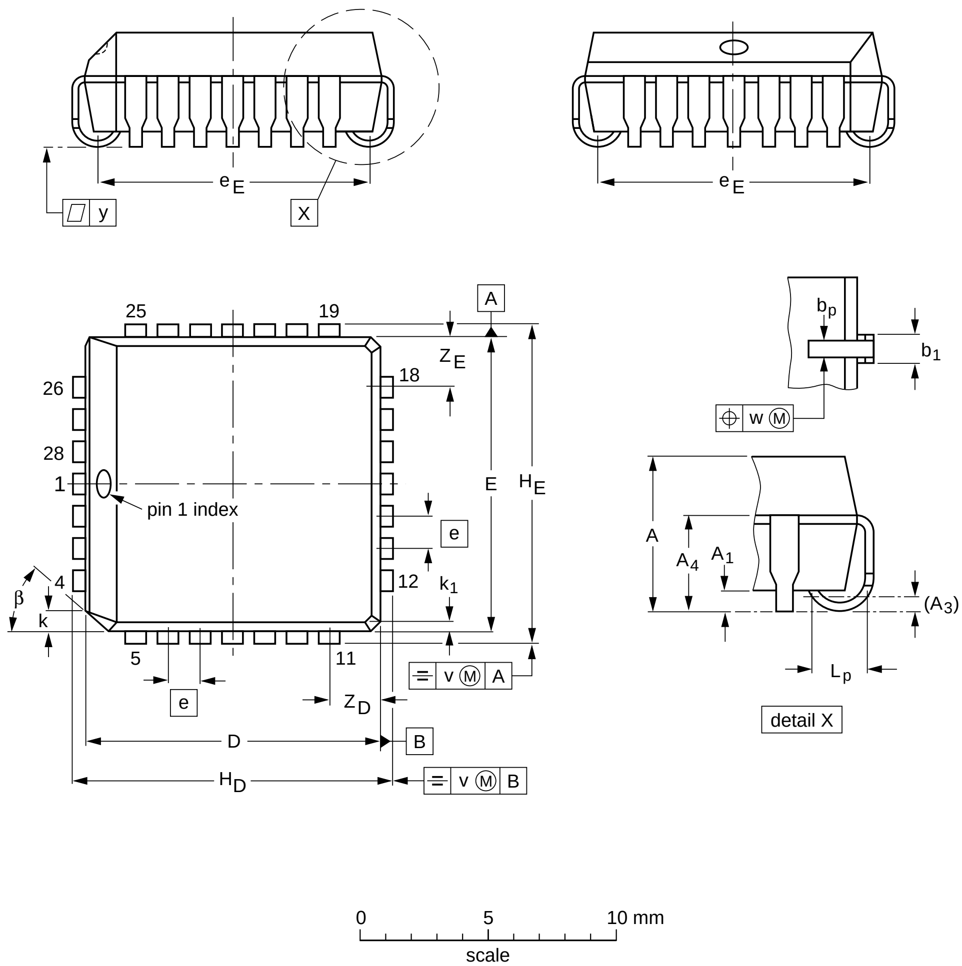
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**

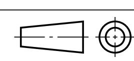


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	D(1)	E(1)	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	Z_D(1) max.	Z_E(1) max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-2						~~92-11-17~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

PLCC

REFLOW SOLDERING

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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